HPS TRIGGER

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HPS trigger

Trigger system:

- Electromagnetic calorimeter :556 channels
- Muon system: 144 channels
- Silicon-Vertex tracker will not participate in the trigger
- Test run trigger system : 440 EC channels

What will Trigger do ?

- Find the clusters in the EC calorimeter
- Select at least two clusters in opposite quadrants of the EC calorimeter
- Apply the energy cuts
  - E1, E2 > Emin (depends on the beam energy)
  - E1+E2< Emax (depends on the beam energy)

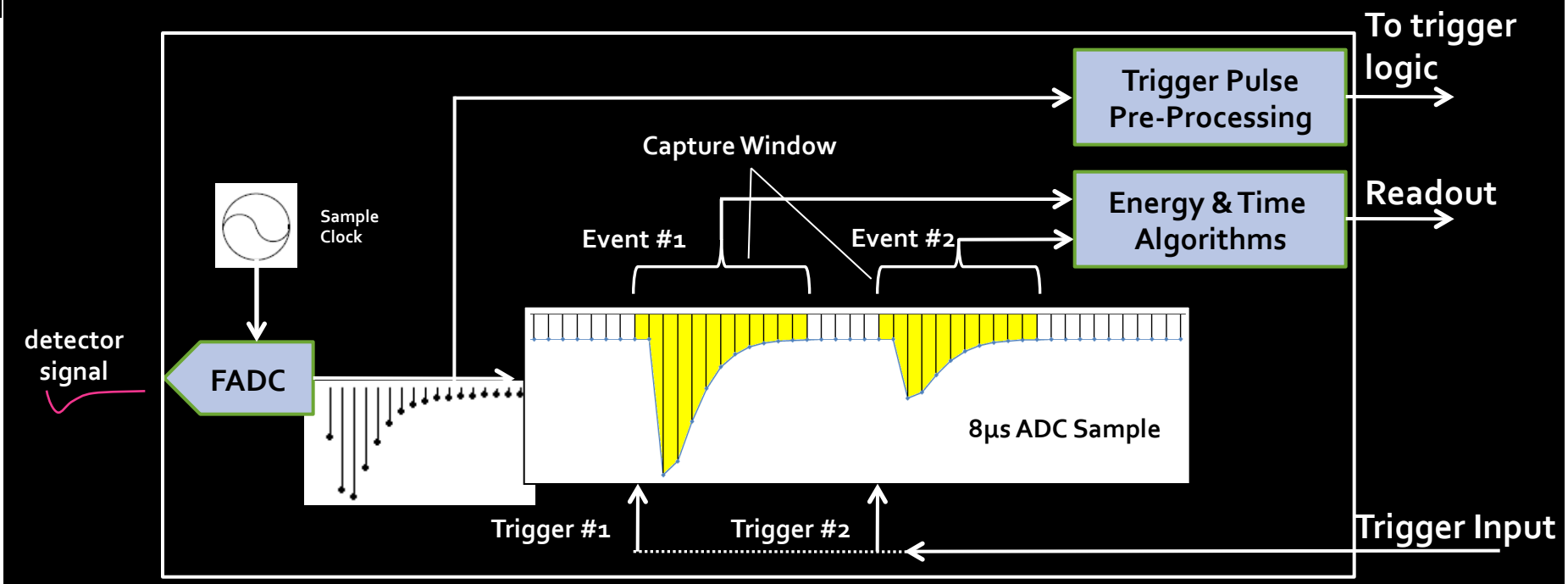
Level 1 Trigger

- The maximum trigger decision time (latency) is set to 3 μs for level 1
- The first stage of the trigger logic is incorporated into the FADC
- Crate Trigger Processors (CTP) will perform cluster finding
- Sub System Processor (SSP) will form the final decision
- The system is free running and driven by a (16/32/64) ns global clock.
- The trigger system is nearly deadtimeless.
- The maximum trigger accept rate is 50 KHz.

Front end electronics: FADC
(Flash Amplitude to Digital Converter)

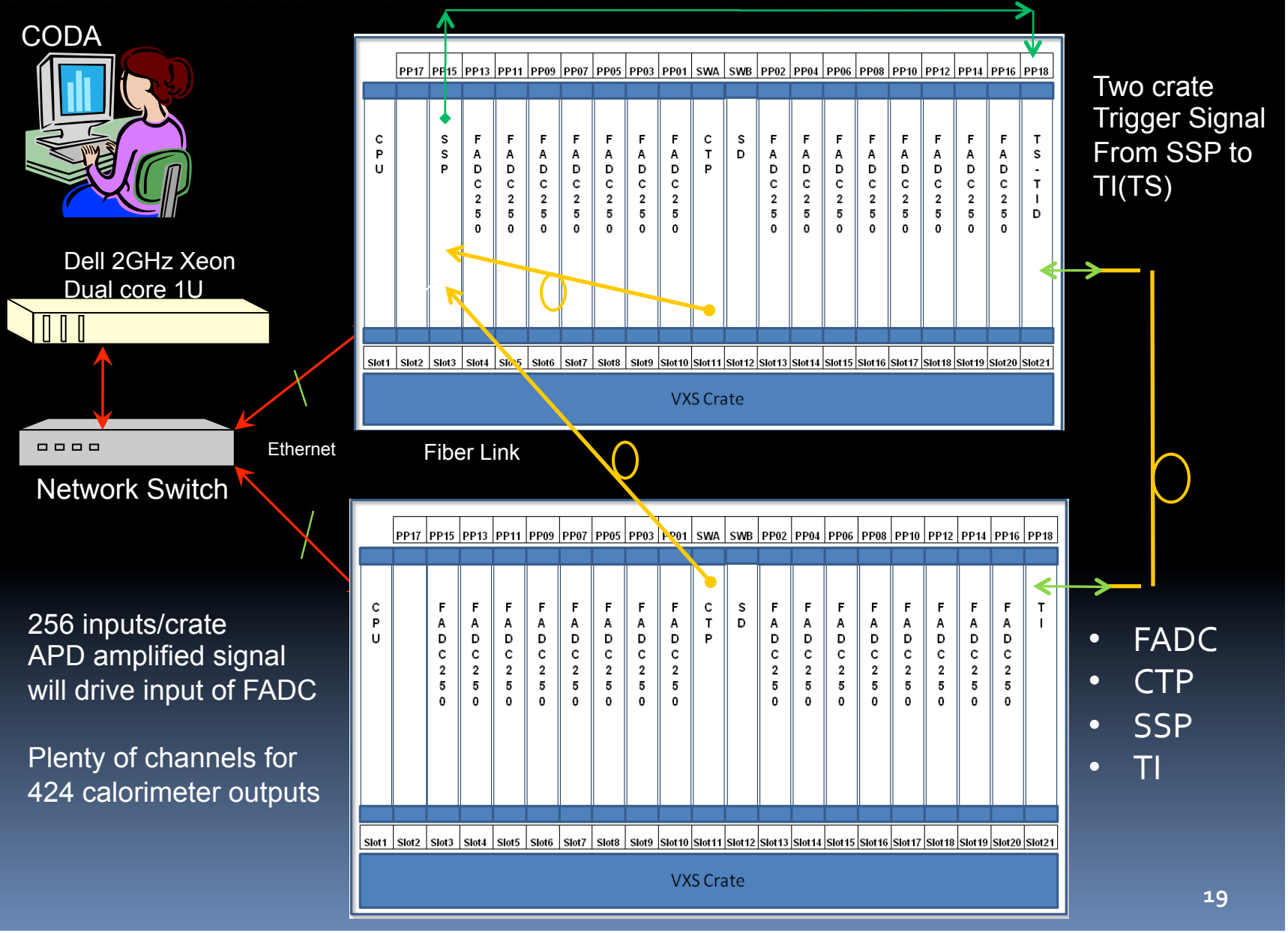
- The 16-channel Jlab-made 12 bits 250 MHz
- The FADCs will send information to the Crate Trigger Processor (CTP) board installed in the same crate.
- From our proposal: "FADC will be in production by the end of 2010 calendar year".
- Still waiting…
- Critical delivery date – August 2011.

Flash ADC Implementation



- The clock frequency is 250 MHz, 4ns
- FADC will integrate the signal N1 clocks before and N2 clocks after the threshold
- The signal information will include energy sum and timing .
- Info will be sent to CTP board over the back-plane serial bus every ?? ns
- We will request to implementation of scalers in every FADC channel for monitoring.

TEST RUN DAQ AND TRIGGER



256 inputs/crate
APD amplified signal
will drive input of FADC

Plenty of channels for
424 calorimeter outputs

- FADC
- CTP
- SSP
- TI

Requirements for Trigger Hardware

From Chris's report:

- **Requirements** for readout electronics and trigger hardware
  - Expected signal rates (MC trigger simulation group ?)
  - Expected signal amplitudes/pulse widths (that we know from the previous experiments)
  - Expected trigger rates (MC, still in progress)
  - Channel sum resolution → 6 bits proposed, 8 ns. Is this acceptable? (MC group again)
  - FADC scalers ? (Probably yes)
- **Firmware development can begin once requirements are complete. (June 2011)**
  - Must create realistic work plan for firmware on FADC250, CTP and SSP

Report Time	Bits	Energy, bits	Time, bits	Time accuracy
4 ns	1	1	0	4 ns
8 ns	2	1	1	4 ns
16 ns	4	2	2	4 ns
32 ns	8	5	3	4 ns
32 ns	8	6	2	8 ns
64 ns	16	12	4	4 ns

Back up Solutions

If FADCs and other trigger logic blocks will not be delivered in time we need to find out the back up solution for the test run in 2012.

1. Buy CAEN FADCs and CAEN trigger boards V1495 ($300K)

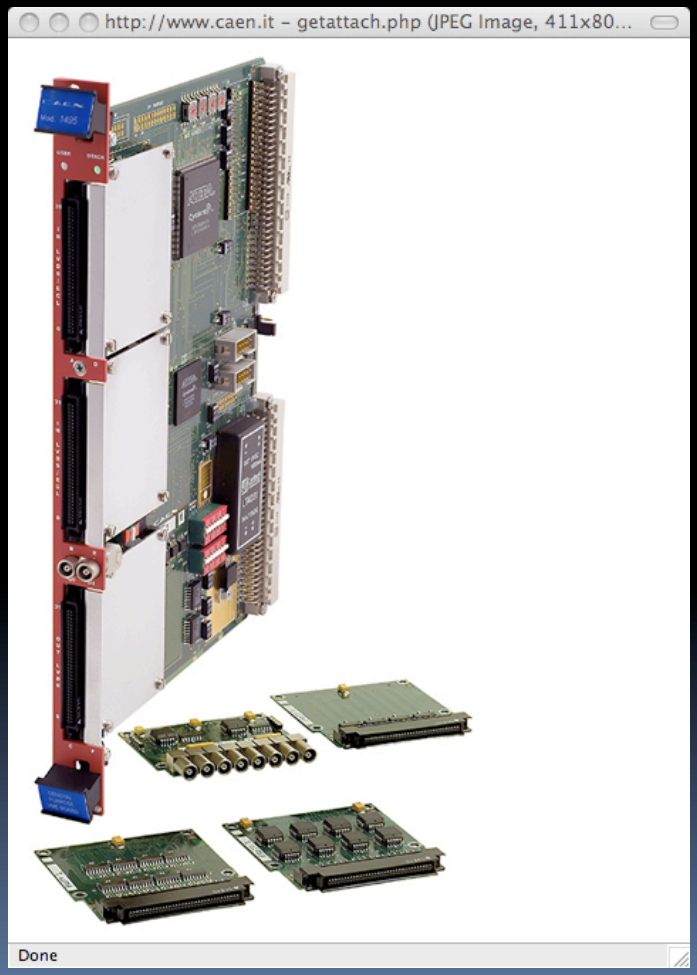
2. Use existing CLAS Trigger DAQ with gated ADCs

- Jlab-made discriminators have two outputs with two independent thresholds: one for TDC (low threshold) and one for the trigger (high threshold)
- Cluster finding will be done on the base of hit based information (yes/no, no energy measurements)
- The threshold value will play role of the energy cut off for the clusters
- There is a possibility to use the total energy sum from the different quadrants in the trigger
- This system was used in the previously conducted dvcs experiments and photoproduction experiments

DVCS Trigger Logic

- dvcs Trigger Logic was based on the Field-Programmable Gate Array (FPGA)
- Commercially available CAEN Module V1495 is a VME board, suitable for various digital Gate/Trigger/Translator/Buffer/Test applications, which can be directly customized by the User.

CAEN Module V1495



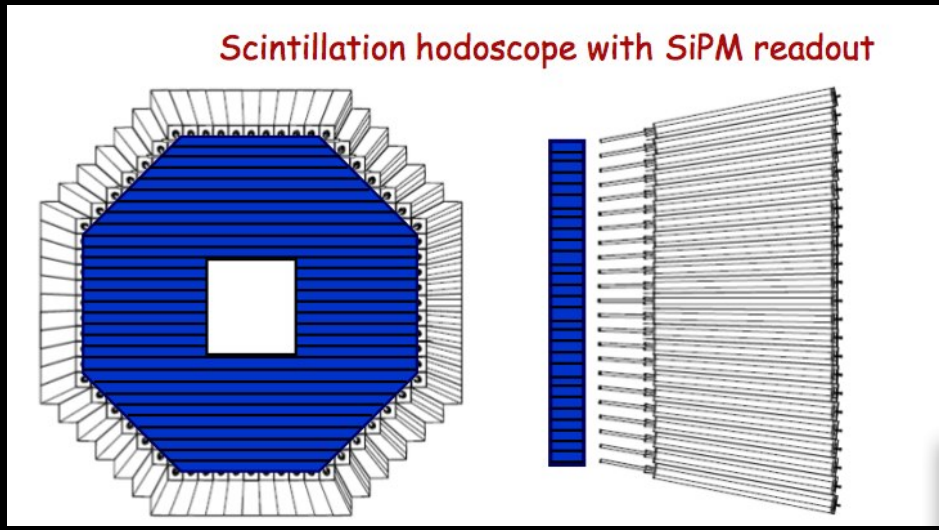
- 64 inputs, expandable to 162 (with 32 outputs)
- 32 outputs, expandable to 130 (with 64 inputs)
- This module was used in the previous CLAS experiments

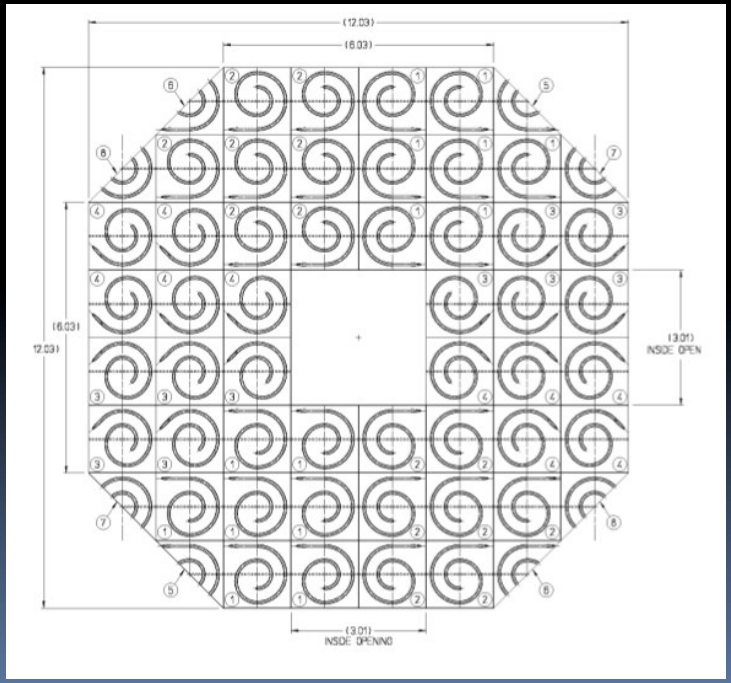
DVCS Trigger configuration

- 424 Internal Calorimeter (IC) signals
- 72 hodoscope signals
- 6 TOF (OR of all counters in each sector)
- 6 CC inputs (OR of all counters in each sector)
- 4x6=24 EC inputs (inner and total energy threshold signals in each sector)
- 532 input signals in total

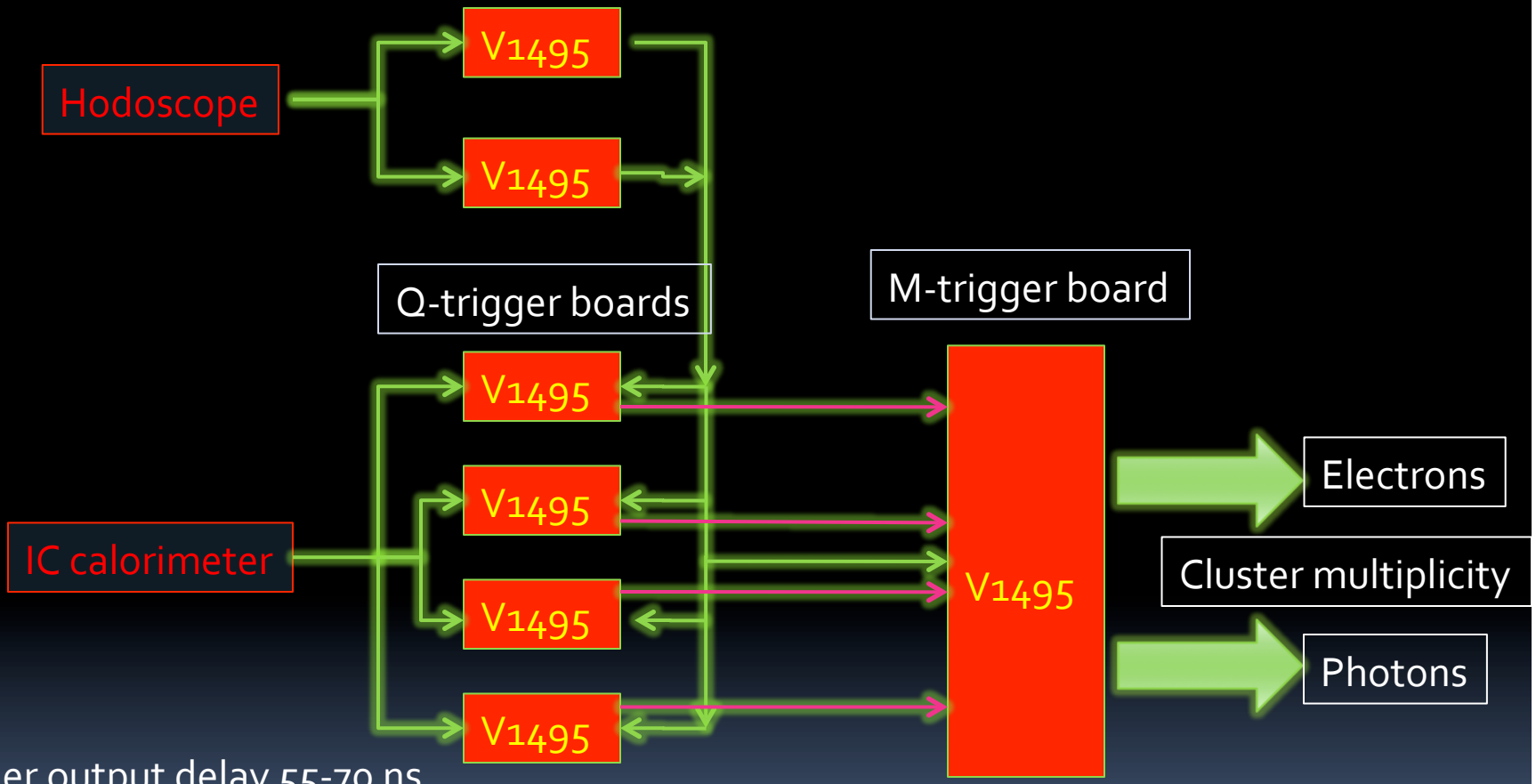
IC Hodoscope

- Pixels of 1 cm scintillator plates
- 3.8x3.8 cm^2 dimension
- Total number of pixels 56
- Total number of readout channels 72
- Silicon PMT readout





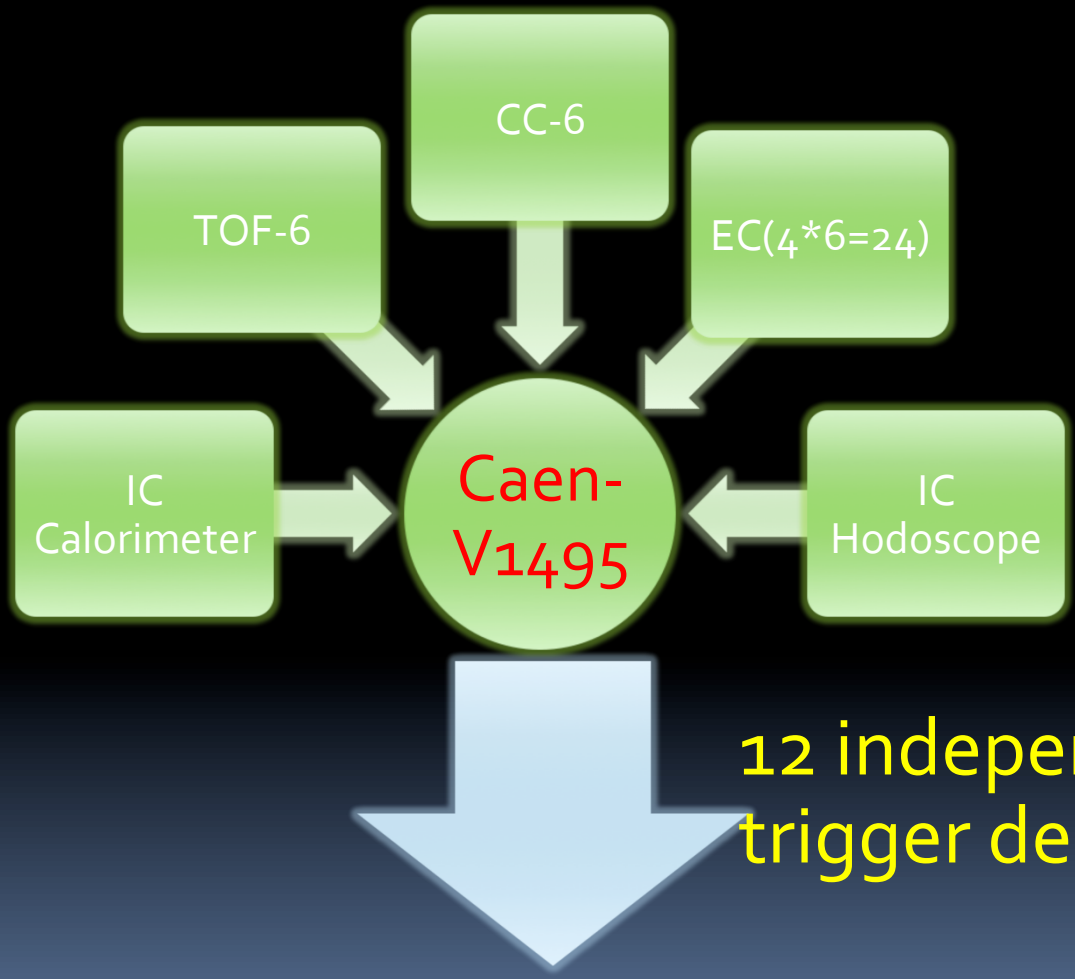
IC-Hodoscope Trigger Logic



- Trigger output delay 55-70 ns
- Programmable cluster definition in a 3x3 window: 1-9 hits
- Cluster peak detection algorithm

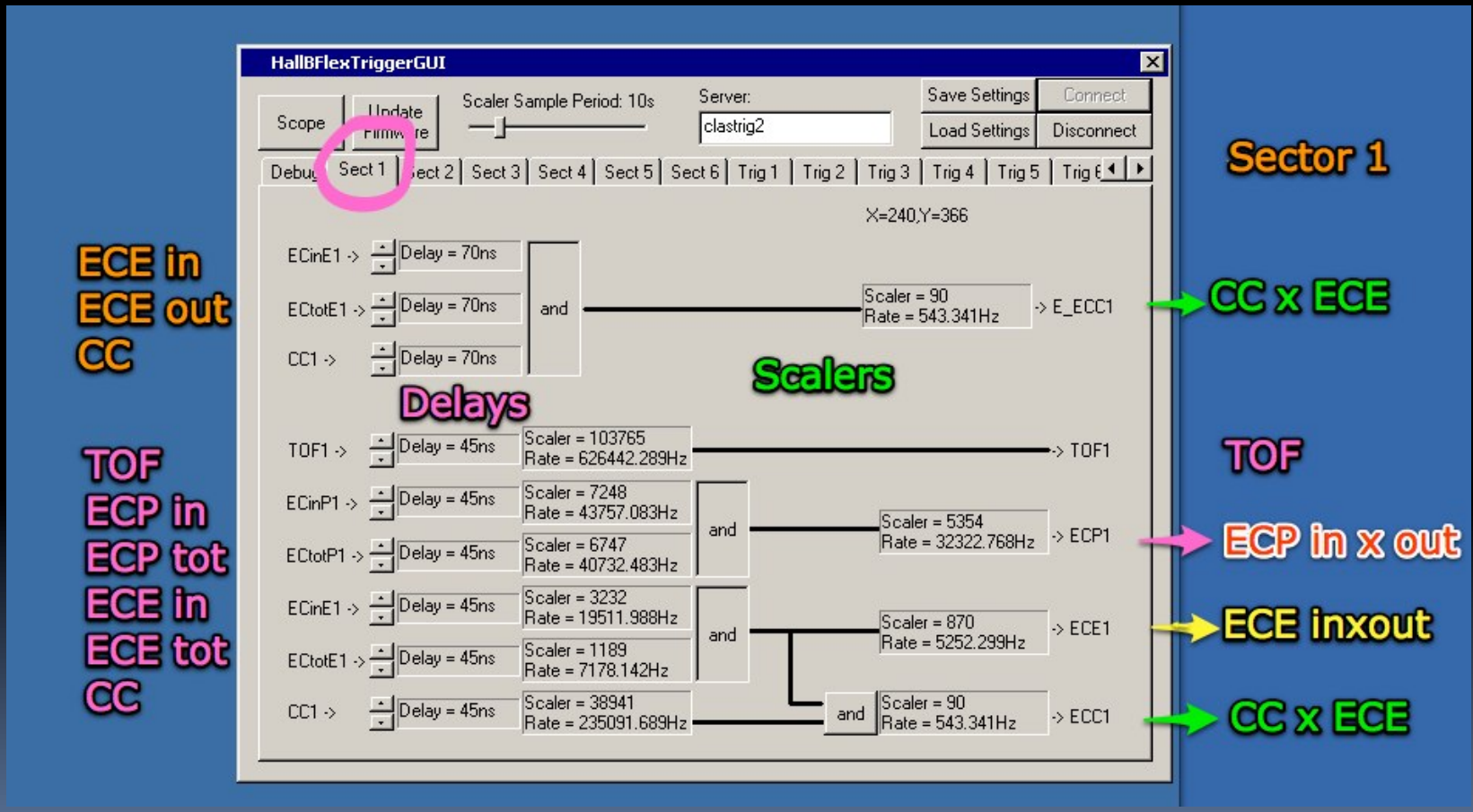
'Electron'= ICxHodo
'Photon '= IC only

General trigger scheme

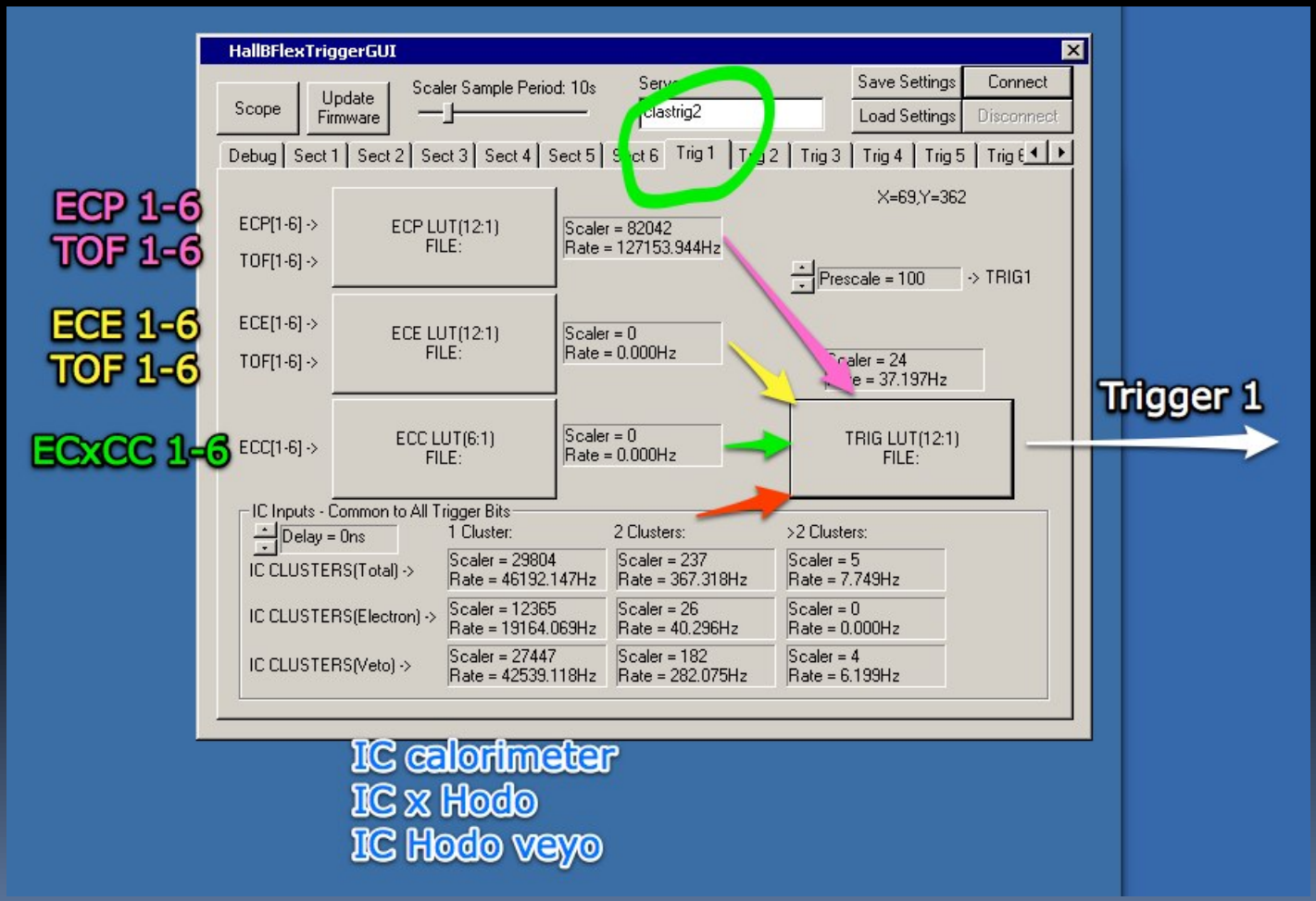


12 independent trigger decisions

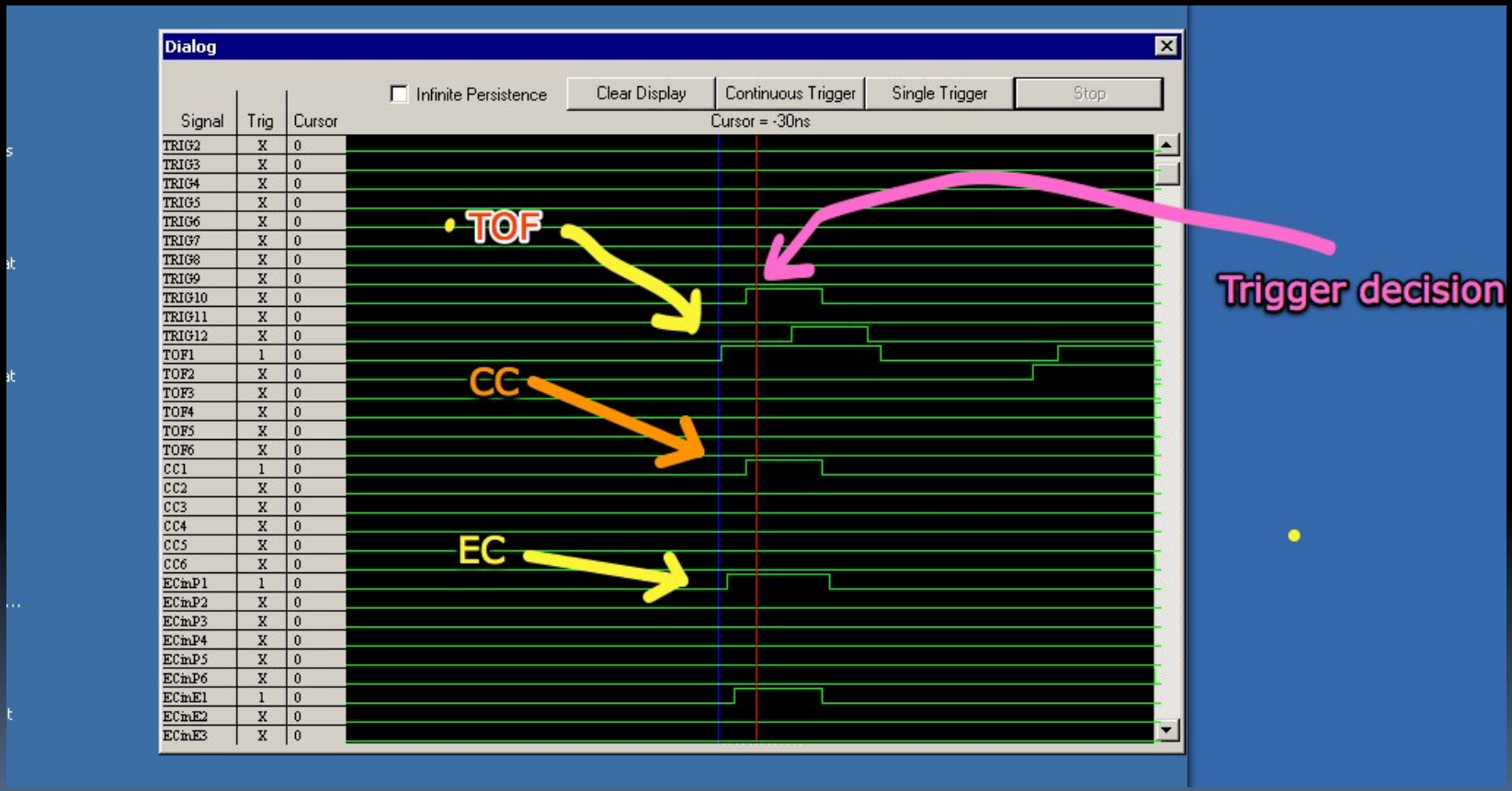
Sector Based Trigger GUI



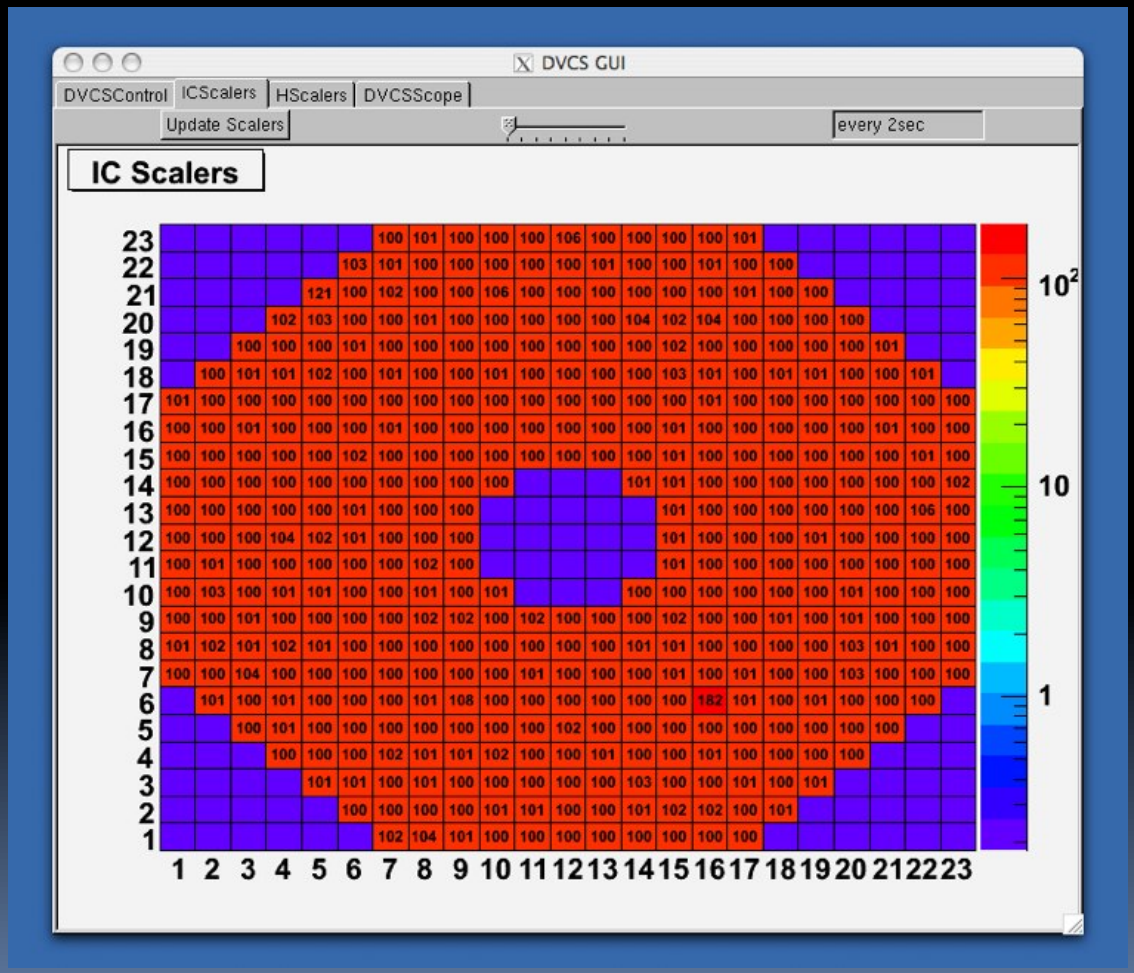
Main Trigger GUI



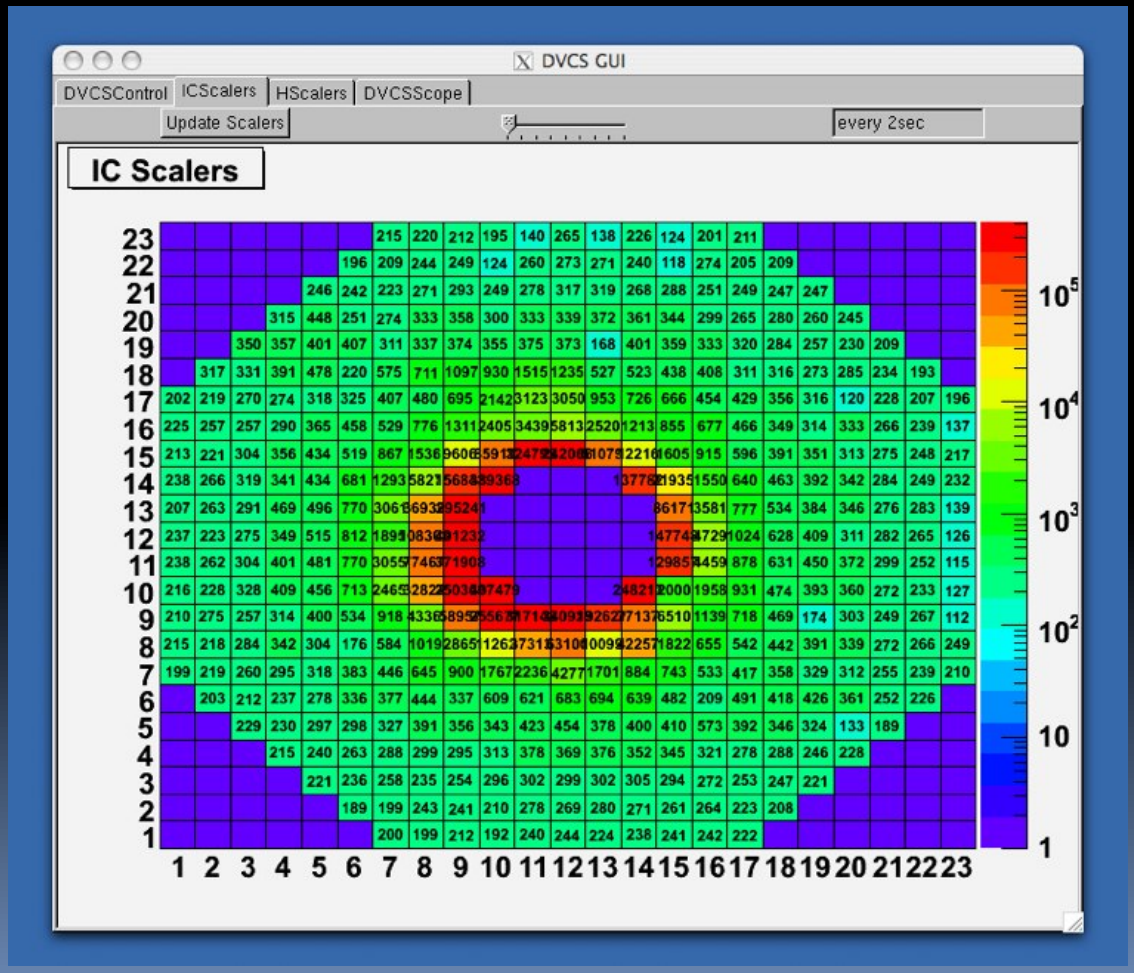
Scope Display



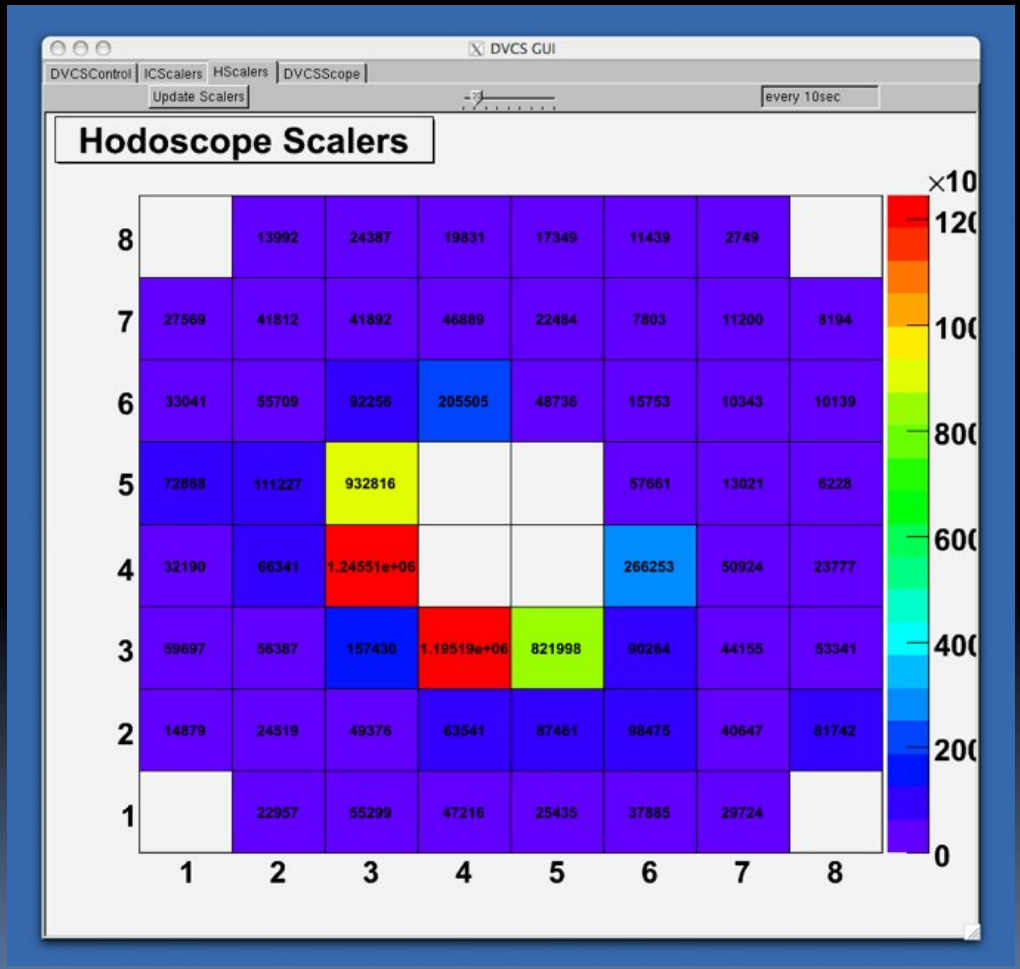
IC Calorimeter Laser Scalers



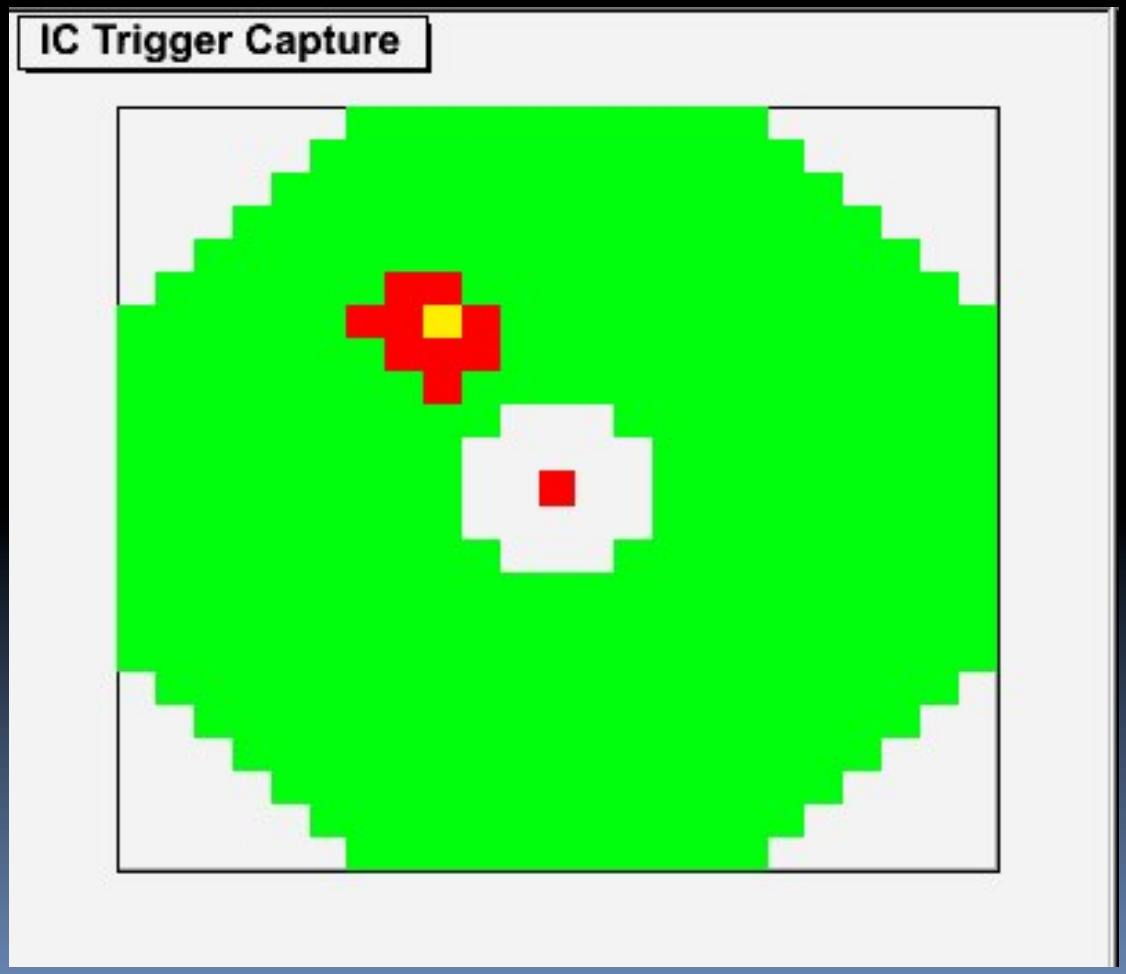
IC Calorimeter Scalers with Beam



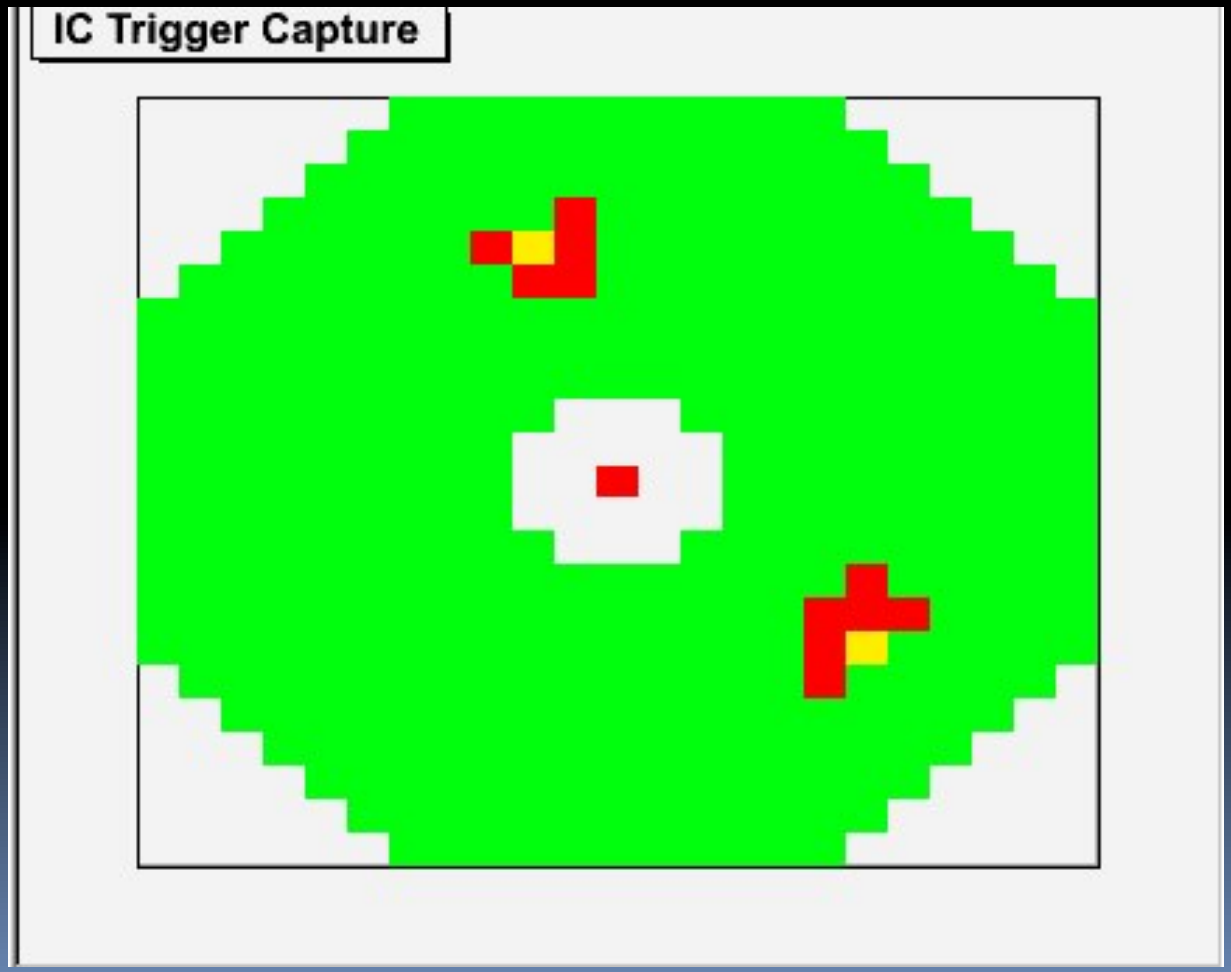
IC Hodoscope with Beam



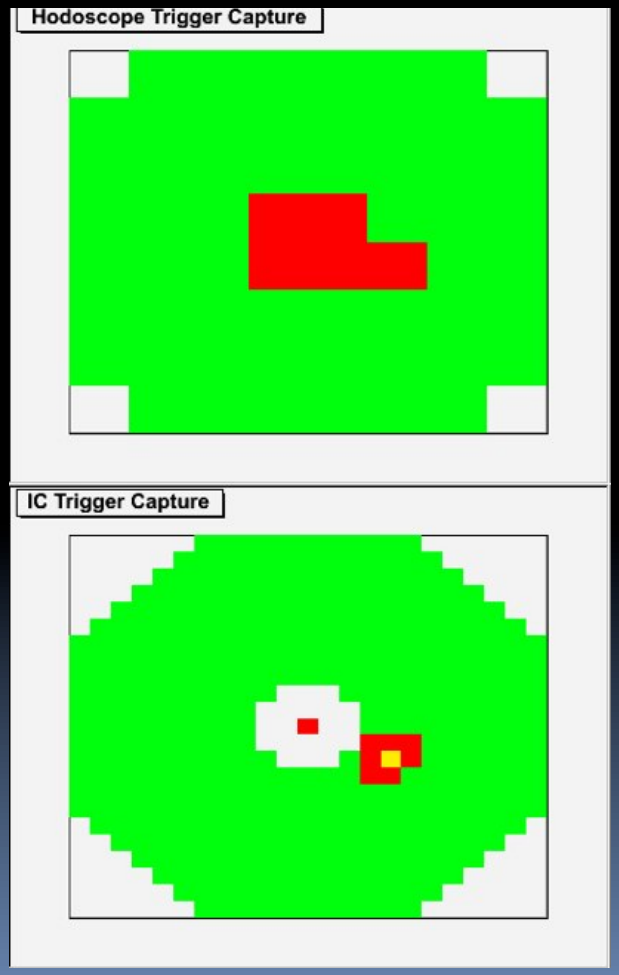
Selected by IC trigger: One Cluster Event



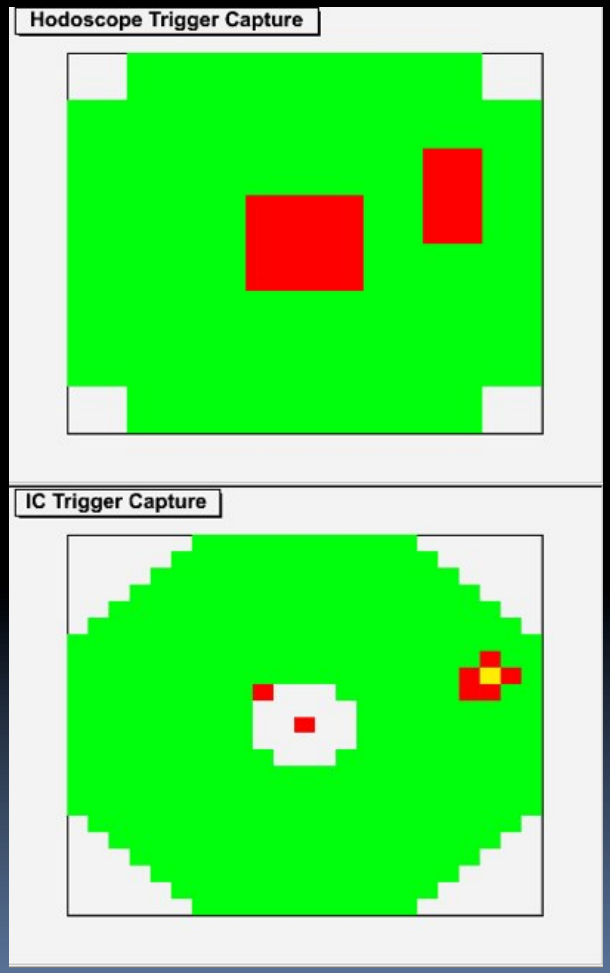
Selected by IC trigger Two Clusters Event



One Cluster Event in Coincidence with Hodoscope



One Cluster Event in Coincidence with Hodoscope



Conclusion

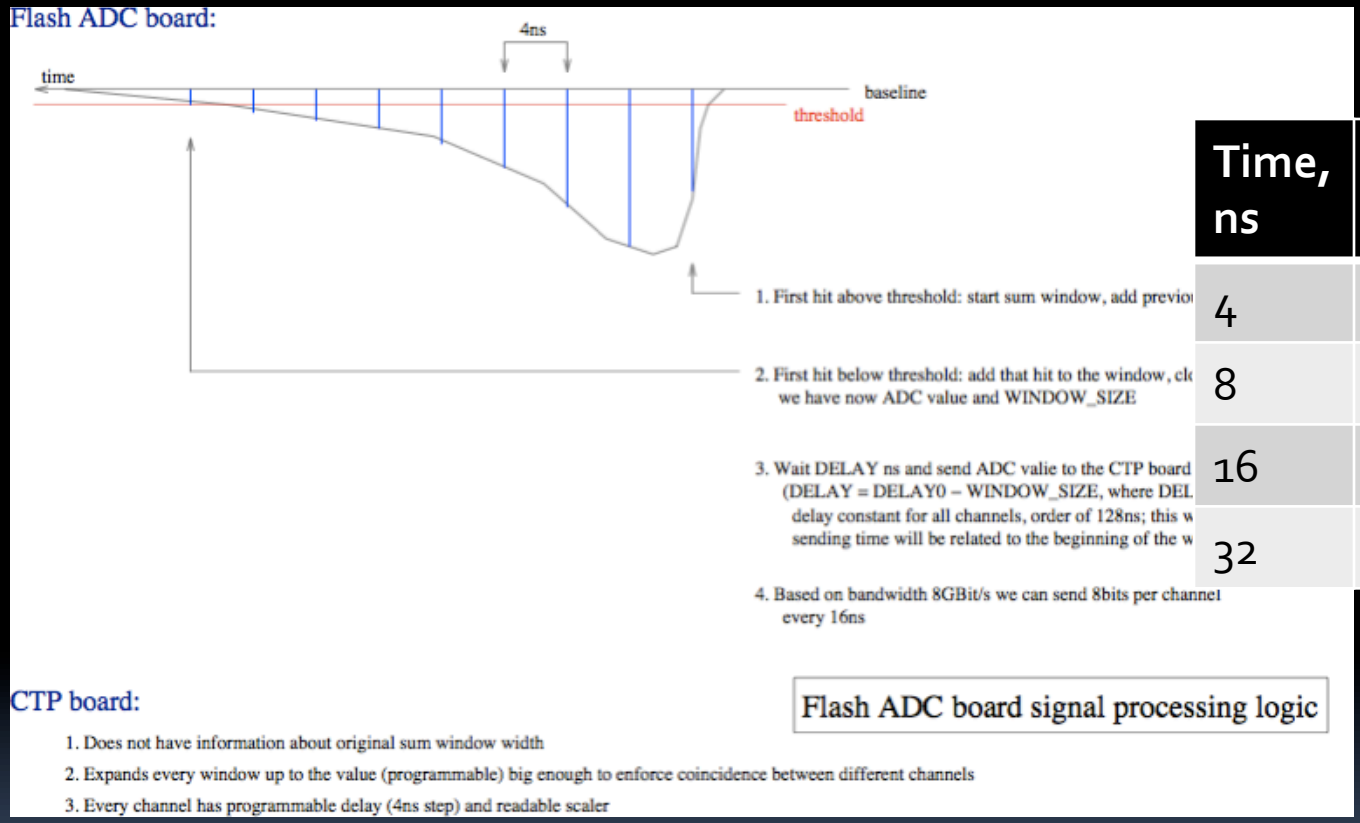
- Hardware status
  - We have VXS crates, CTP, SSP and TI
  - We are waiting for the delivery of FADC in June
- Firmware development will start in June-August
- However we need to prepare the back up plan for test run in case of the technical problems with trigger electronics.

END

Activities to be completed

- **Define requirements** for readout electronics and trigger hardware
  - Expected signal rates
  - Expected signal amplitudes/pulse widths
  - Expected trigger rates
  - Calorimeter APD channels only? Or are there Hodoscope channels?
  - Channel sum resolution → 6 bits proposed. Is this acceptable?
- **Firmware development can begin once requirements are complete. (June 2011)**
  - Must create realistic work plan for firmware on FADC250, CTP and SSP
  - Plan must account for simulation and testing
- **Hardware Status**
  - We have VXS crates, **C**rate **T**rigger **P**rocessors, **S**ub**S**ystem Processor, **T**rigger **I**nterface **S**ignal **D**istribution and **R**ead-**O**ut **C**ontrollers
  - 35 FADC250 are presently at the assembly company and delivery is imminent
  - FADC250 will need acceptance testing and then will be fully qualified in a two crate test (Summer 2011)

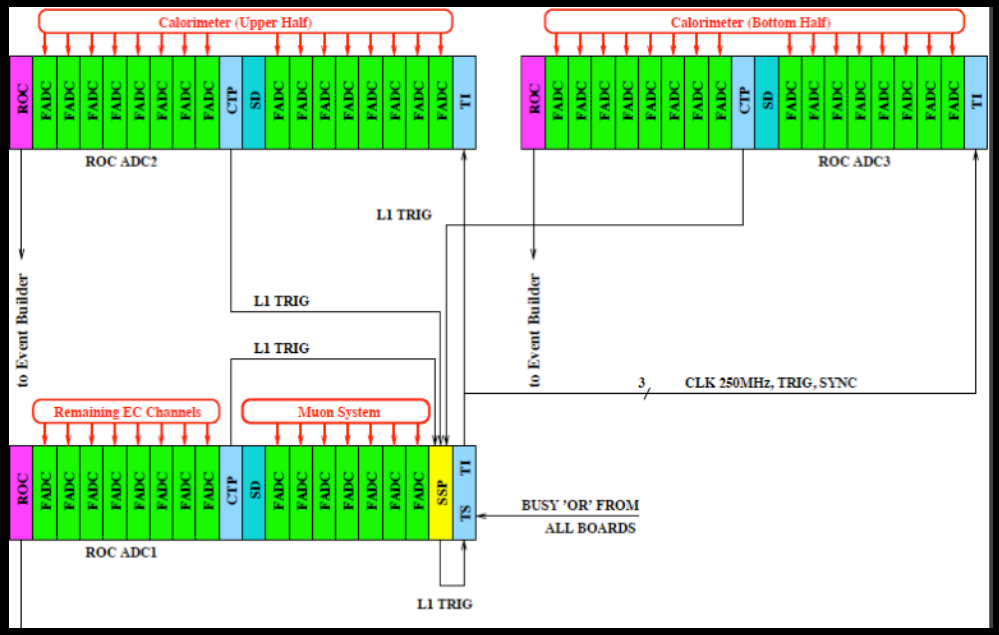
Signal processing on the FADC



Time, ns	Bits	Energy+ Time, bits
4	1	1+0
8	2	1+1
16	4	2+2
32	8	5+3

- FADC will integrate the signal N1 clocks before and N2 clocks after the threshold
- The signal information will include energy sum (5 bits) and timing (3 bits, 4ns resolution).
- Info will sent to Crate Tr. Processor CTP board over the back-plane serial bus every 32 ns
- We hope to have scalers in every FADC channel for monitoring.

DAQ and trigger



- FADC
- Crate Trigger Processor (CTP)
- Sub System Processor (SSP)
- Trigger Interface (TI)

- The FADCs send signal information to CTP
- The signal information will include energy and timing info for every channel
- Information will be sent to the CTP board every 32 ns.
- The CTP board will perform cluster finding and form the trigger decision.
- Results are reported to Sub System Processor , SSP
- The SSP board forms the final trigger decision
- All crates receive the 250-MHz master clock

General scheme

- Sector based logic
- Central trigger unit